Amendments to the Drawings:

The attached replacement sheet of drawing includes changes to Fig. 2 and replaces the original sheet including Fig. 2.

In Figure 2, the legend --Prior Art-- was added.

Attachments following last page of this Amendment:

Replacement Sheet (1 page)
Annotated Sheet Showing Change(s) (1 page)

REMARKS

Claims 1-15 and 23-37 were pending as of the office action mailed on August 7, 2006. Claims 1 and 23 have been amended. No new matter has been added. Applicant respectfully requests reconsideration in view of the foregoing amendments and these remarks.

I. Interview Summary

Applicant thanks the Examiner for the courtesy of a telephone interview conducted on September 19, 2006. In the interview, Applicant and the Examiner discussed the Anzai reference (United States Patent No. 6,898,722). Applicant respectfully asserted that Anzai shows multiple signal lines with different signaling modalities. In some signal modalities a high clock signal is provided for a limited duration of time after data transmission (see Fig. 5, and associated text at cols. 6-7). On at least one signal path, the odd-numbered data signal path, a pulse signal is provided to signal the end of transmission.(See again Fig. 5.) No agreement was reached.

II. Drawing Objections

The Examiner objects to the drawings, suggesting that Fig. 2 should be designated by a legend such as --Prior Art--. Applicant has amended Fig. 2 as requested by the Examiner. No new matter has been added.

III. Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 7 and 29 are merely objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

IV. Claim Rejections under 35 U.S.C. §102

Claims 1-3, 5-6, 11-14, 23-25, 27-28 and 33-36 were rejected as allegedly being anticipated by U.S. Patent No. 6,898,722 ("Anzai"). Applicant respectfully traverses the rejection.

a. Claim 1 and its dependent claims

Claim 1 recites a circuit that includes a clock transmitter in communication with a clock bus, a clock receiver in communication with the clock bus, and a driver in communication with

the clock bus. The driver drives and maintains a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

Anzai is directed to a data transfer method and system of DDR divided data. The Examiner suggests that Applicant's claimed clock transmitter is found within Anzai's sending unit 100; that Applicant's claimed clock receiver is found within Anzai's receiving unit 200; and that Applicant's claimed driver is Anzai's output circuit 109. Applicant respectfully disagrees. Applicant respectfully asserts that Anzai fails to teach or suggest, at least, a driver in communication with the clock bus that is operable to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

Anzai's system includes three signal lines that transfer odd-numbered divided data, even-numbered divided data, and a transfer clock signal from the sending unit to the receiving unit in parallel. (Col. 5, lines 37-42). The receiving unit captures the odd-numbered data at each leading edge of the transfer clock and captures the even-numbered data at each trailing edge. (Col. 5, lines 43-50). The sending unit appends a 'data output completion signal,' consisting of two pulses, to the odd-numbered data string after transmission is complete. (Col., 5, lines 54-58; Abstract). The sending unit also fixes the transfer clock signal to HIGH for a period of time that corresponds to the duration of this completion signal. (Col., 5, lines 51-54; Abstract). When the transfer clock is kept at the HIGH level during a period from the leading to the trailing edge of the odd-numbered data – that is, when the clock is kept HIGH during the completion signal – the receiving unit recognizes that transmission is complete, and latches the captured data. (Col. 5, lines 59-62). Thereafter, the transfer clock is transitioned to a low, disabled state.

Applicant respectfully asserts that Anzai fails to teach or suggest, at least, a driver to drive and maintain a voltage of a clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus. The Examiner suggests that Applicant's claimed first voltage level is the level associated with Anzai's data output completion signal. Applicant respectfully disagrees.

Figure 5 shows that Anzai's completion signal is transferred on a data bus, not on a clock bus. Accordingly, Applicant respectfully asserts for at least this reason alone, claim 1 is allowable over Anzai.

Further, Applicant respectfully asserts that Anzai does not teach or suggest maintaining a voltage *of a clock bus* to a first voltage level while the clock transmitter is not transmitting. As discussed above, Anzai does include a clock signal path that is used to provide the transfer clock signal. Anzai's sending unit holds the transfer clock signal to HIGH only for a period of time that corresponds to the duration of the completion signal. (Col. 5, lines 51-54). The sending unit then transitions the clock signal to a *second* voltage level, as shown in Figures 2 and 5, after the completion signal is transmitted. In other words, the clock signal is not maintained at the same voltage level after the completion signal is transmitted. Anzai therefore teaches away from claim 1, which recites a driver operable to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus. Accordingly, Applicant respectfully asserts that claim 1 is allowable over Anzai.

Claims 2-3, 5-6 and 11-14 depend from claim 1 and are allowable for at least the same reasons set forth above with respect to claim 1.

b. Claim 23 and its dependent claims

Claim 23 recites a circuit that includes a clock signal transmission means in communication with a clock bus, a clock signal receiving means in communication with the clock bus, and a voltage driving means in communication with the clock bus. The voltage driving means drives and maintains a voltage of the clock bus to a first voltage level while the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

Claim 23 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 24-25, 27-28 and 33-36 depend from claim 23 and are allowable for at least the same reasons set forth above with respect to claim 23.

V. Claim Rejections under 35 U.S.C. §103

The Examiner has not established that Anzai teaches or suggests every limitation of Applicant's claimed invention. In particular, as discussed above, Anzai fails to teach or suggest, at least, a driver to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus. The additional references cited by the Examiner do not cure this deficiency.

c. Claims 4 and 26

Claims 4 and 26 were rejected as allegedly being unpatentable over Anzai in view of U.S. Patent No. 5,732,249 ("Masuda"). Applicant respectfully traverses this rejection.

Claim 4 depends from claim 1 and is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 26 depends from claim 23 and is allowable for at least the same reasons set forth above with respect to claim 23.

d. Claims 8-10 and 30-32

Claims 8-10 and 30-32 were rejected as allegedly being unpatentable over Anzai in view of U.S. Patent No. 5,355,468 ("Jeppesen"). Applicant respectfully traverses this rejection.

Claims 8-10 depend from claim 1 and are allowable for at least the same reasons set forth above with respect to claim 1.

Claims 30-32 depend from claim 23 and are allowable for at least the same reasons set forth above with respect to claim 23.

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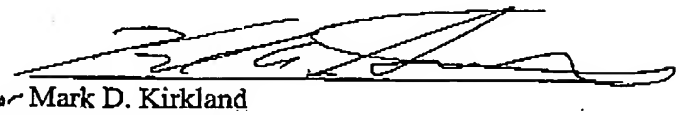
VI. Conclusion

Applicant petitions for an extension of time to respond to the instant action up to and including December 7, 2006. Enclosed is a credit card authorization for a one-month extension of time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 12-7-06



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